

TPS63025x High Current, High Efficiency Single Inductor Buck-Boost Converter

1 Features

- Real Buck or Boost operation with automatic and seamless transition between Buck and Boost operation
- 2.3V to 5.5V input voltage range
- 2A Continuous Output Current : $V_{IN} \geq 2.7V$, $V_{OUT} = 3.3V$
- Adjustable and fixed output voltage
- Efficiency up to 95% in Buck or Boost mode and up to 97% when $V_{IN} = V_{OUT}$
- 2.5MHz typical switching frequency
- 35 μ A operating quiescent current
- Integrated Soft –Start
- Power Save Mode
- True shutdown function
- Output capacitor discharge function
- Over-Temperature Protection and Over current Protection
- Wide capacitance selection
- Small 1.766 mm x 2.086mm, 20-pin WCSP

2 Applications

- Cellular Phones, Smart Phones
- Tablets PC
- PC and Smart Phone accessories
- Point of load regulation
- Battery Powered Applications

3 Description

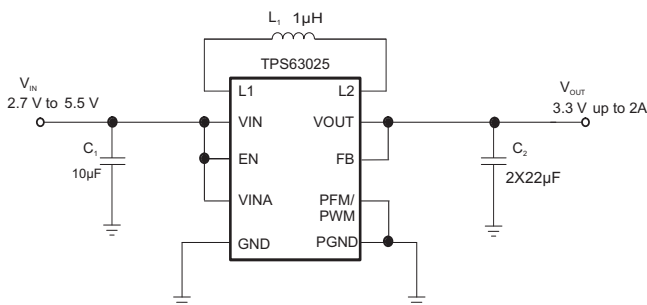
The TPS63025 are high efficiency, low quiescent current buck-boost converters suitable for application where the input voltage is higher or lower than the output. Output currents can go as high as 2A in boost mode and as high as 4A in buck mode. The maximum average current in the switches is limited to a typical value of 4A. The TPS63025 regulates the output voltage over the complete input voltage range by automatically switching between buck or boost mode depending on the input voltage ensuring a seamless transition between modes. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain highest efficiency. At low load currents, the converter enters Power Save Mode to maintain high efficiency over the complete load current range. There is a PFM/PWM pin that allows the user to choose between automatic PFM/PWM mode operation and forced PWM operation. During PWM mode a fixed-frequency of typically 2.5MHz is used. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 20-pin WCSP package measuring 1.766 mm x 2.086mm.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS630250	DSBGA (20)	1.766 mm x 2.086 mm
TPS630251		
TPS630252		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application



Efficiency vs Output Current

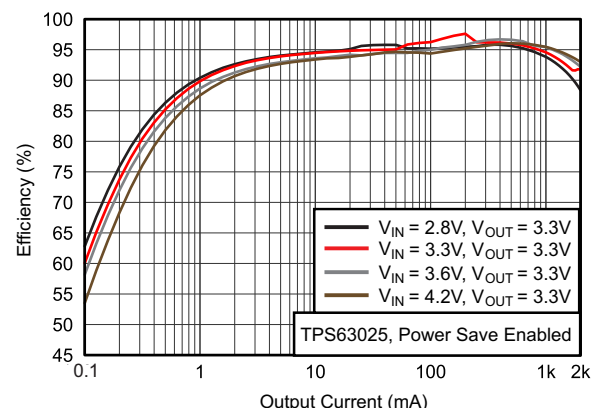


Table of Contents

1	Features	1	9.3	Feature Description.....	11
2	Applications	1	9.4	Device Functional Modes.....	14
3	Description	1	10	Application and Implementation	15
4	Typical Application	1	10.1	Application Information.....	15
5	Revision History	2	10.2	Typical Application	15
6	Device Comparison Table	3	11	Power Supply Recommendations	20
7	Pin Configuration and Functions	3	12	Layout	20
8	Specifications	4	12.1	Layout Guidelines	20
8.1	Absolute Maximum Ratings	4	12.2	Layout Example	20
8.2	Handling Ratings	4	12.3	Thermal Information.....	20
8.3	Recommended Operating Conditions.....	4	13	Device and Documentation Support	21
8.4	Thermal Information	4	13.1	Device Support	21
8.5	Electrical Characteristics.....	5	13.2	Documentation Support	21
8.6	Timing Requirements.....	6	13.3	Related Links	21
8.7	Typical Characteristics.....	7	13.4	Trademarks	21
9	Detailed Description	10	13.5	Electrostatic Discharge Caution.....	21
9.1	Overview	10	13.6	Glossary	21
9.2	Functional Block Diagram	10	14	Mechanical, Packaging, and Orderable Information	21

5 Revision History

Changes from Original (May 2014) to Revision A

Page

- | | | |
|---|--|----------|
| • | Changed Header from TPS63025 to TPS630250, TPS630251, TPS630252 part numbers | 1 |
| • | Changed Load Regulation Typ spec from "125 mV/A" to "2.5 mV/A" | 5 |

6 Device Comparison Table

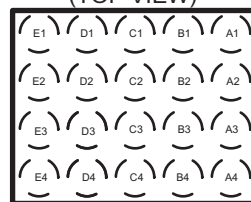
PART NUMBER ⁽¹⁾	VOUT
TPS630250YFF	Adjustable
TPS630251YFF	2.9V
TPS630252YFF	3.3V

(1) For all available packages, see the orderable addendum at the end of the datasheet.

7 Pin Configuration and Functions

**WCSP
20-Pin
YFF**

(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1,A2,A3	PWR	Buck-boost converter output
FB	A4	IN	Voltage feedback of adjustable version, must be connected to VOUT on fixed output voltage versions
L2	B1,B2,B3	PWR	Connection for Inductor
PFM/PWM	B4	IN	set low for PFM mode, set high for forced PWM mode. It must not be left floating
PGND	C1,C2,C3	PWR	Ground for Power stage
GND	C4	PWR	Ground for Control stage
L1	D1,D2,D3	PWR	Connection for Inductor
EN	D4	IN	Enable input. Set high to enable and low to disable. It must not be left floating.
VIN	E1,E2,E3	PWR	Supply voltage for power stage
VINA	E4	PWR	Supply voltage for control stage.

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage ⁽²⁾	L2 ⁽³⁾ , VOUT, FB	-0.3	4	V
	VIN, L1 ⁽³⁾ , EN, VINA, PFM/PWM	-0.3	7	V
Input current	Continuous average current into L1 ⁽⁴⁾		2.7	A
Operating junction temperature, T _J		-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are DC-voltages with respect to ground terminal.
- (3) L2, L1 voltage can exceed Absolute Maximum ratings during normal operation. As long as the device is operated within recommend operating conditions device reliability is not affected.
- (4) Maximum continuous average input current 3.5A, under those condition do not exceed 105°C for more than 25% operating time.

8.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	700	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions⁽¹⁾

		MIN	TYP	MAX	UNIT
VIN	Input Voltage Range	2.3		5.5	V
VOUT	Output Voltage	2.3		3.6	V
L	Inductance ⁽²⁾	0.5	1	1.3	μH
C _{out}	Output Capacitance ⁽³⁾	20			μF
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating virtual junction temperature	-40		125	°C

- (1) Refer to the Application Information section for further information
- (2) Effective inductance value at operating condition. The nominal value given matches a typical inductor to be chosen to meet the inductance required.
- (3) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the nominal capacitor required with the dc bias effect for this type of cap. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS63025x YFF 20 PINS	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	53.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.5	
R _{θJB}	Junction-to-board thermal resistance	10.1	
Ψ _{JT}	Junction-to-top characterization parameter	1.4	
Ψ _{JB}	Junction-to-board characterization parameter	9.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

$T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY							
V_{IN}	Input voltage range		2.3		5.5	V	
V_{IN_Min}	Minimum input voltage to turn on into full load	$I_{OUT}=2A$		2.8		V	
I_{OUT}	Continuous Output Current ⁽¹⁾			2		A	
I_Q	Quiescent current	V_{IN}	$I_{OUT}=0mA$, $EN=V_{IN}=3.6V$, $V_{OUT}=3.3V$ $T_J=-40^\circ\text{C}$ to 85°C , not switching		35	70	μA
		V_{OUT}				12	μA
I_{sd}	Shutdown current	$EN=low$, $T_J=-40^\circ\text{C}$ to 85°C		0.1	2	μA	
UVLO	Under voltage lockout threshold	V_{IN} falling	1.6	1.7	1.9	V	
	Under voltage lockout hysteresis			180		mV	
	Thermal shutdown	Temperature rising		140		$^\circ\text{C}$	
	Thermal Shutdown hysteresis			20		$^\circ\text{C}$	
LOGIC SIGNALS EN, PFM/PWM							
V_{IH}	High level input voltage	$V_{IN}=2.3V$ to $5.5V$	1.2			V	
V_{IL}	Low level input voltage	$V_{IN}=2.3V$ to $5.5V$			0.4	V	
I_{ikg}	Input leakage current	$EN=GND$ or V_{IN}		0.01	0.2	μA	
OUTPUT							
V_{OUT}	Output Voltage range		2.3		3.6	V	
V_{FB}	TPS630250 Feedback regulation voltage			0.8		V	
V_{FB}	TPS630250 Feedback voltage accuracy ⁽²⁾	PWM mode	-1%		1%		
V_{FB}	TPS630250 Feedback voltage accuracy ⁽²⁾	PFM mode	-1%	1.3%	+3%		
V_{OUT}	TPS630251 Output voltage accuracy ⁽²⁾	PWM mode	2.871	2.9	2.929	V	
V_{OUT}	TPS630251 Output voltage accuracy ⁽²⁾	PFM mode	2.871	2.938	2.987	V	
V_{OUT}	TPS630252 Output voltage accuracy ⁽²⁾	PWM mode	3.267	3.3	3.333	V	
V_{OUT}	TPS630252 Output voltage accuracy ⁽²⁾	PFM mode	3.267	3.343	3.399	V	
$I_{PWM/PFM}$	Output current to enter PFM mode	$V_{IN}=3V$; $V_{OUT}=3.3V$		350		mA	
I_{FB}	Feedback input bias current	$V_{FB}=0.8V$		10	100	nA	
$R_{DS_Buck(on)}$	High side FET on-resistance	$V_{IN}=3.0V$, $V_{OUT}=3.3V$		35		m Ω	
	Low side FET on-resistance	$V_{IN}=3.0V$, $V_{OUT}=3.3V$		50		m Ω	
$R_{DS_Boost(on)}$	High side FET on-resistance	$V_{IN}=3.0V$, $V_{OUT}=3.3V$		25		m Ω	
	Low side FET on-resistance	$V_{IN}=3.0V$, $V_{OUT}=3.3V$		50		m Ω	
I_{IN}	Average input current limit ⁽³⁾	$V_{IN}=3.0V$, $V_{OUT}=3.3V$ $T_J=65^\circ\text{C}$ to 125°C	3.5	4.5	5	A	
f_s	Switching Frequency			2.5		MHz	
R_{ON_DISC}	Discharge ON-Resistance	$EN=low$		120		Ω	
	Line regulation	$V_{IN}=2.8V$ to $5.5V$, $I_{OUT}=2A$		7.4		mV/ V	
	Load regulation	$V_{IN}=3.6V$, $I_{OUT}=0A$ to $2A$		2.5		mV/ A	

(1) For minimum and maximum output current in a specific working point see Figure 1 and Equation 1 through Equation 4.

(2) Conditions: $L=1\ \mu\text{H}$, $C_{OUT}=2 \times 22\ \mu\text{F}$.

(3) For variation of this parameter with Input voltage and temperature see Figure 1.

8.6 Timing Requirements

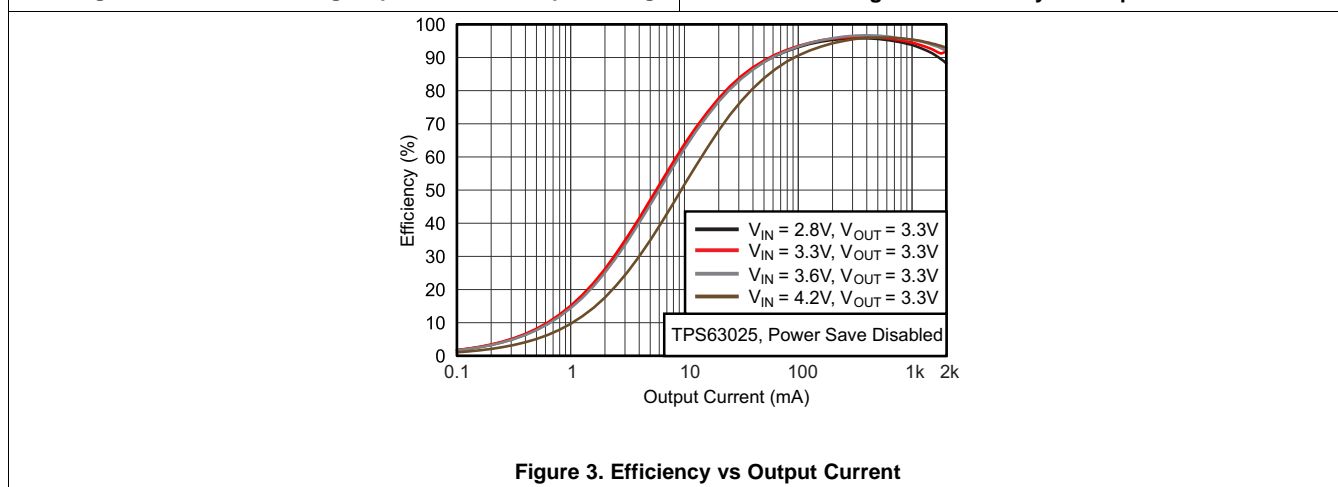
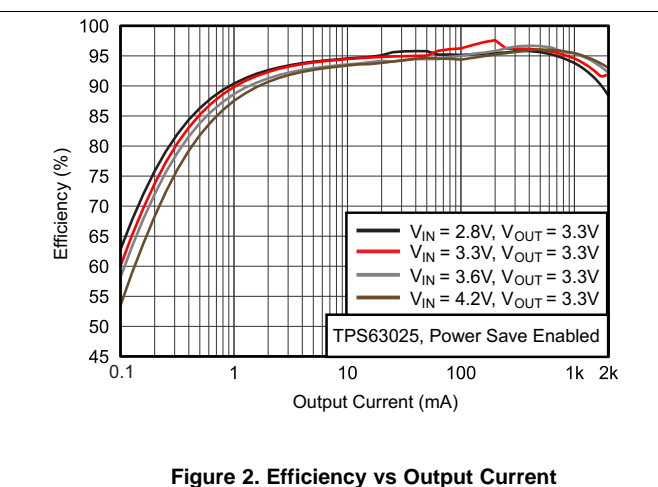
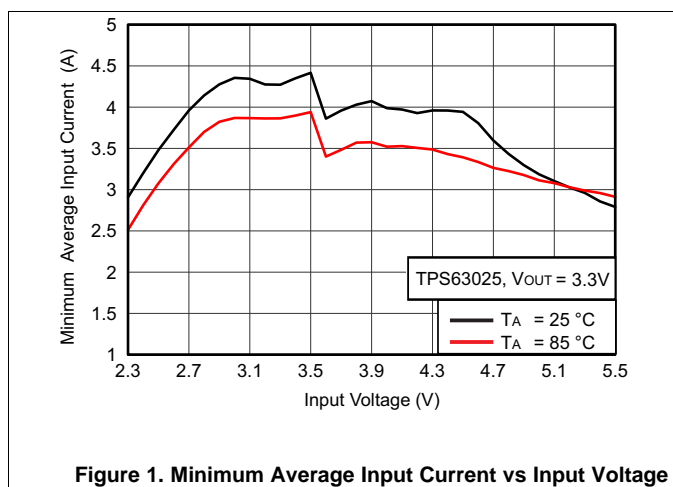
$T_J = -40^{\circ}\text{C}$ to 125°C , typical values are at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
t_{SS}	Soft-start time	$V_{OUT} = \text{EN} = \text{low to high}$, Buck mode $V_{IN} = 3.6\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 2\text{A}$		450		μs
		$V_{OUT} = \text{EN} = \text{low to high}$, Boost mode $V_{IN} = 2.8\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 2\text{A}$		700		μs
t_d	Start up delay	Time from when EN=high to when device starts switching		100		μs

8.7 Typical Characteristics

Table 1. Table Of Graphs

DESCRIPTION		FIGURE
Minimum average input current	vs Input voltage (TPS63025, $V_{OUT} = 3.3V$)	Figure 1
Efficiency	vs Output current (TPS63025, Power Save Enabled, $V_{OUT} = 3.3V$)	Figure 2
	vs Output current (TPS63025, Power Save Disabled, $V_{OUT} = 3.3V$)	Figure 3
	vs Output current (TPS63025, Power Save Enabled, $V_{OUT} = 2.9V$)	Figure 4
	vs Output current (TPS63025, Power Save Disabled, $V_{OUT} = 2.9V$)	Figure 5
	vs Input voltage (TPS63025, Power Save Enabled, $V_{OUT} = 3.3V$, $I_{OUT} = \{10mA; 20mA; 1A; 2A\}$)	Figure 6
	vs Input voltage (TPS63025, Power Save Disabled, $V_{OUT} = 3.3V$, $I_{OUT} = \{10mA; 20mA; 1A; 2A\}$)	Figure 7
	vs Input voltage (TPS63025, Power Save Enabled, $V_{OUT} = 2.9V$, $I_{OUT} = \{10mA; 20mA; 1A; 2A\}$)	Figure 8
	vs Input voltage (TPS63025, Power Save Disabled, $V_{OUT} = 2.9V$, $I_{OUT} = \{10mA; 20mA; 1A; 2A\}$)	Figure 9
Output voltage	vs Output current (TPS63025, $V_{IN} = 2.8V, 3.3V, 3.6V, 4.2V$, $V_{OUT} = 3.3V$)	Figure 10
	vs Output current (TPS63025, $V_{IN} = 2.8V, 3.3V, 3.6V, 4.2V$, $V_{OUT} = 3.3V$)	Figure 11



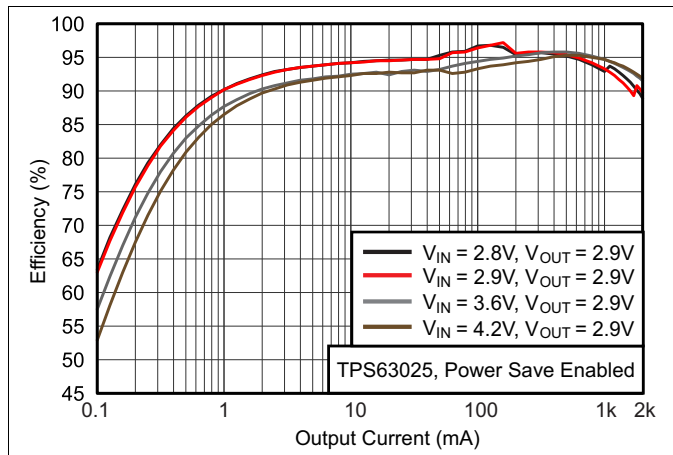


Figure 4. Efficiency vs Output Current

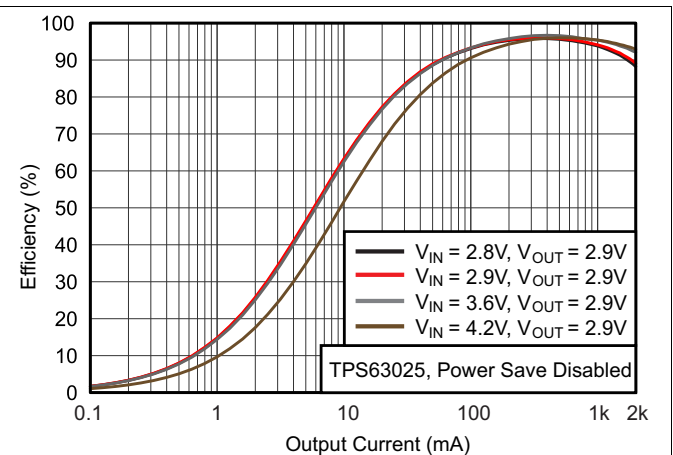


Figure 5. Efficiency vs Output Current

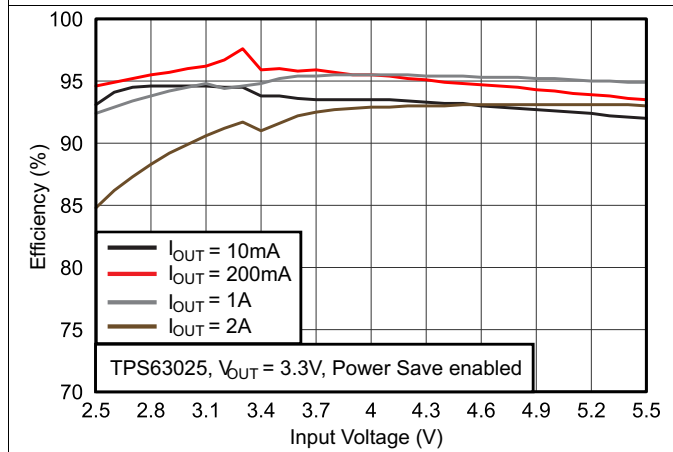


Figure 6. Efficiency vs Input Voltage

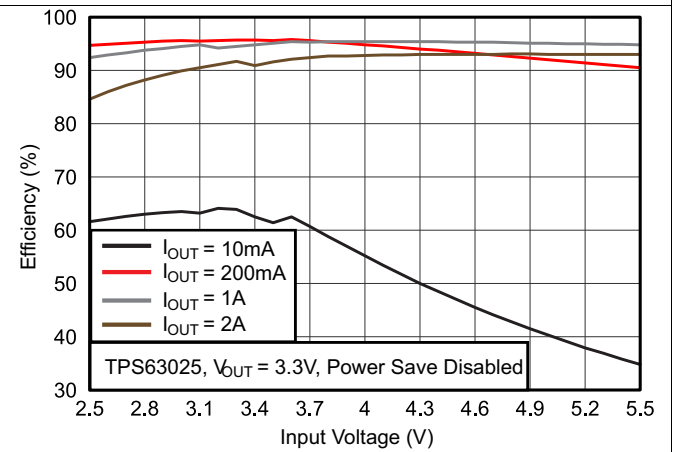


Figure 7. Efficiency vs Input Voltage

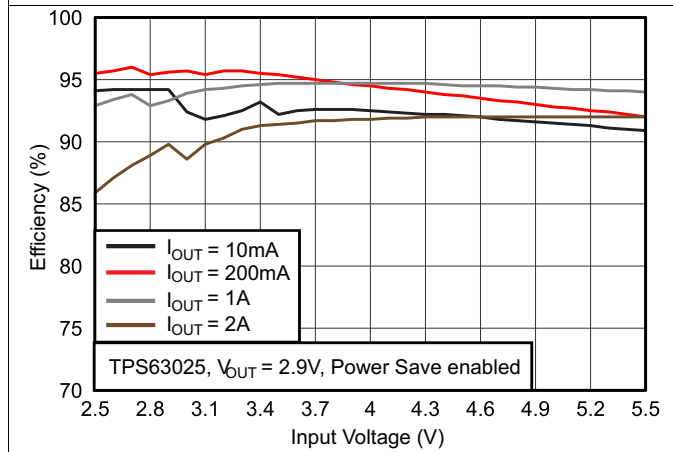


Figure 8. Efficiency vs Input Voltage

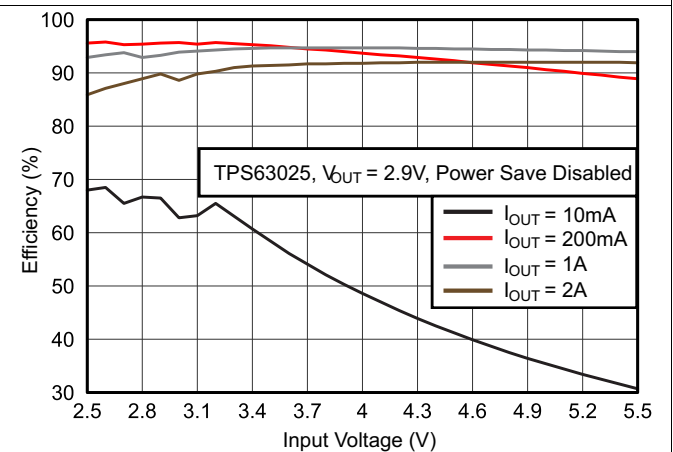


Figure 9. Efficiency vs Input Voltage

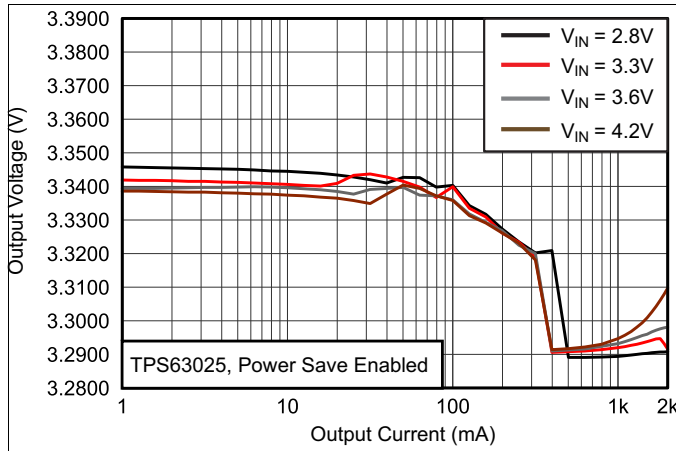


Figure 10. Output Voltage vs Output Current

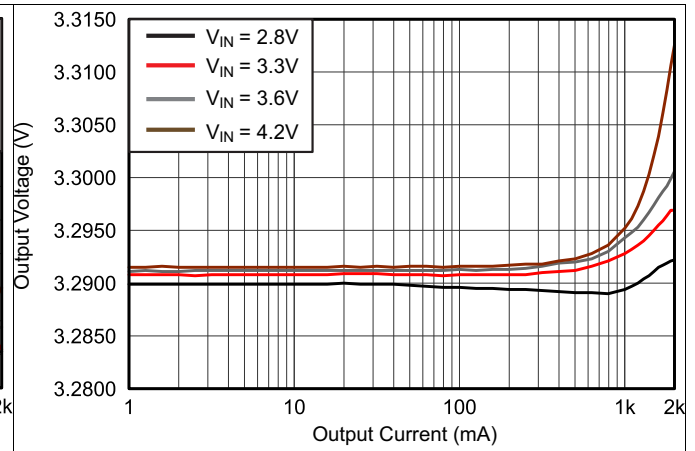


Figure 11. Output Voltage vs Output Current

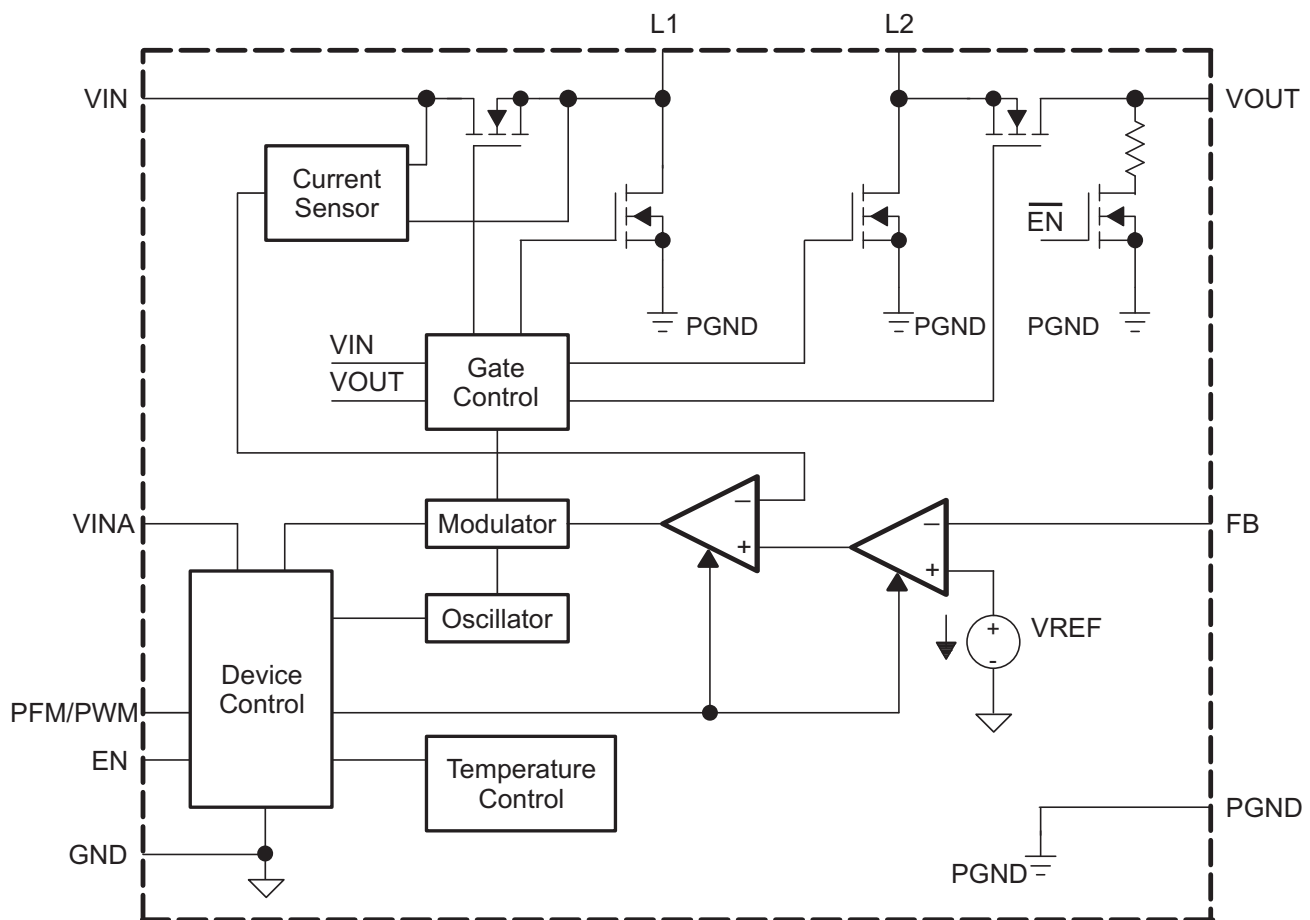
9 Detailed Description

9.1 Overview

The TPS63025 use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over the complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch is held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

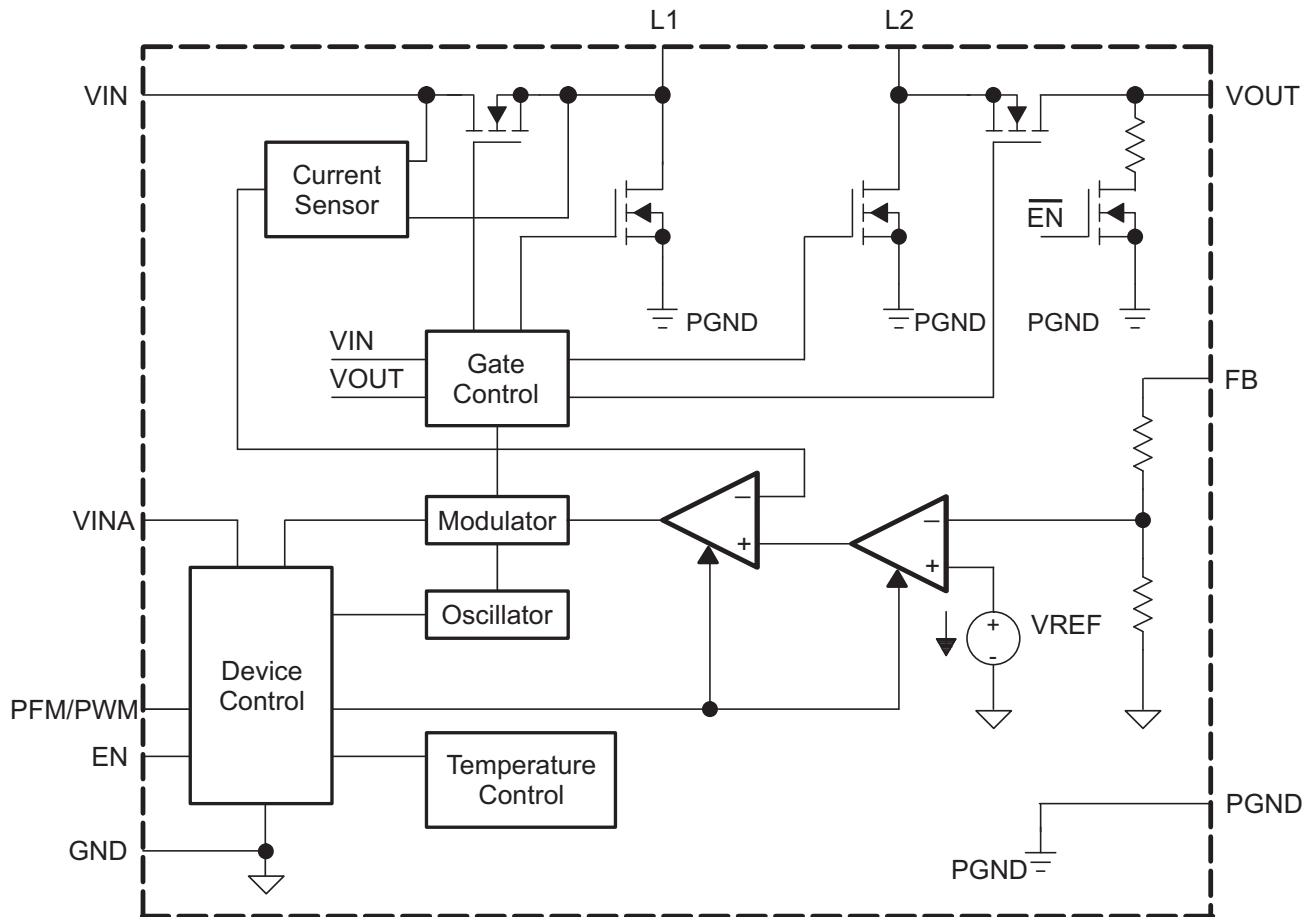
The device provides a seamless transition from buck to boost or from boost to buck operation.

9.2 Functional Block Diagram



Functional Block Diagram (Adjustable Output Voltage)

Functional Block Diagram (continued)



Functional Block Diagram (Fixed Output Voltage)

9.3 Feature Description

9.3.1 Control Loop Description

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 12 shows the control loop.

The non inverting input of the transconductance amplifier, G_{mv} , is assumed to be constant. The output of G_{mv} defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value reached at the end of the on time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the buck or the boost sawtooth ramp. Depending on which of the two ramps the G_{mc} amplified output crosses either the Buck MOSFETs or the Boost MOSFETs will be activated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

Feature Description (continued)

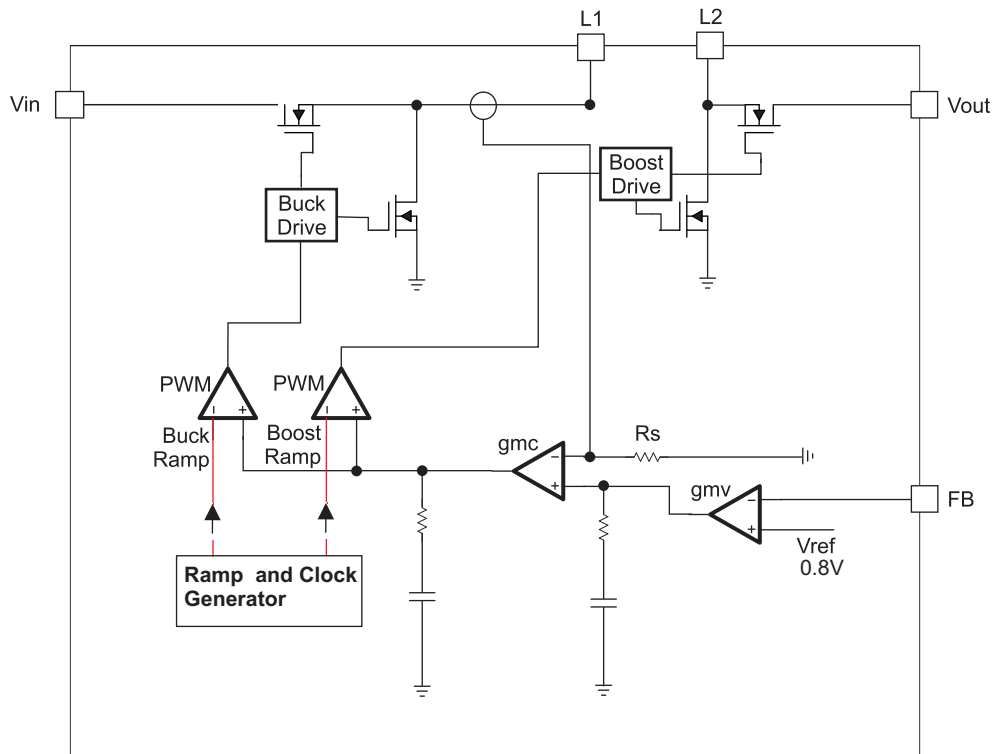


Figure 12. Average Current Mode Control

9.3.2 Device Enable

The device is put into operation when the EN pin is set high. It is put into shutdown mode when the EN pin is set low. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that during shutdown, the output voltage can drop below the input voltage.

9.3.3 Output Discharge Function

When the device is disabled by pulling enable low and the supply voltage is still applied, a transistor is turned on, and discharge the output capacitor. This means, if there is no supply voltage applied the output discharge function is also disabled. The transistor which is responsible of the discharge function, when turned on, operates like an equivalent 120Ω resistor, ensuring typically less than 10ms discharge time for 20μF output capacitance and a 3.3V output.

9.3.4 Soft Start

To minimize inrush current and output voltage overshoot during start up, the device implements a soft start.

At turn on, the input current raises in a controlled manner until the output voltage reaches regulation.

During soft-start, the input current follows the current used to charge an internal soft start capacitor, this creates a linear and controlled increase of Vout.

The soft start time, is measured as the time from when the EN pin is asserted to when the output voltage has reached 90% of it's nominal value. It is typically less than 1ms. There is typically a 100μs delay time from when the EN pin is asserted to when the device starts the switching activity.

The soft start time depends on the load current, the input voltage, and the output capacitor. The soft start time in boost mode is longer then the time in buck mode.

Feature Description (continued)

Thanks to its innovative soft start circuit, the device smoothly ramps up the input current bringing the output voltage to its regulated value without overshoot, even if a large capacitor is connected at the output. This specific case is never confused with a short circuit condition. The inductor current is able to increase and always guarantee soft start unless a real short circuit is applied at the output.

9.3.5 Short Circuit Protection

The TPS63025 provides short circuit protection to protect itself and the application. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and keeps the input current controlled to protect itself and the application. In short circuit, the input current limit is kept at 3A

9.3.6 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN and VINA is lower than its threshold (see electrical characteristics table). When in operation, the device automatically enters shutdown mode if the voltage on VIN and VINA drops below the undervoltage lockout threshold. The device automatically restarts, if the input voltage recovers above the hysteresis amount.

9.3.7 Supply and Ground

The TPS63025 provides two input pins (VIN and VINA) and two ground pins (PGND and GND).

The VIN pin supplies the input power, while the VINA pin provides voltage for the control circuits. A similar approach is used for the ground pins. GND and PGND are used to avoid ground shift problems due to the high currents in the switches. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin.

9.3.8 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

9.3.9 Current Limit

The current limit varies depending on the difference between the input and output voltage. The maximum value of average input current is obtained at the highest difference.

Given the curves provided in Figure 1, it is possible to calculate the output current reached in boost mode, using [Equation 1](#) and [Equation 2](#) and in buck mode using [Equation 3](#) and [Equation 4](#).

$$\text{Duty Cycle Boost} \quad D = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}}} \quad (1)$$

$$\text{Output Current Boost} \quad I_{\text{OUT}} = \eta \times I_{\text{IN}}(1-D) \quad (2)$$

$$\text{Duty Cycle Buck} \quad D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \quad (3)$$

$$\text{Output Current Buck} \quad I_{\text{OUT}} = (\eta \times I_{\text{IN}}) / D \quad (4)$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

I_{IN} = Minimum average input current (Figure 1)

9.4 Device Functional Modes

9.4.1 Power Save Mode Operation

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load currents of approximately 350mA or higher. At lighter loads, the device switches automatically into Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin is used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and lowest supply current to maintain high efficiency. The output voltage is monitored with a comparator at every clock cycle by the thresholds comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the load is still lower than about 350mA, the device switches off again and the same operation is repeated. Instead, if at the next clock cycle, the load is above 350mA, the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only a comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50mV pk-pk, (typically 30mV pk-pk), with 20μF effective output capacitance. In order to avoid a critical voltage drop when switching from 0A to full load, the output voltage in PFM mode is typically 1.3% above the nominal value in PWM mode. Dynamic Voltage Positioning allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode is disabled by setting the PFM/PWM pin high.

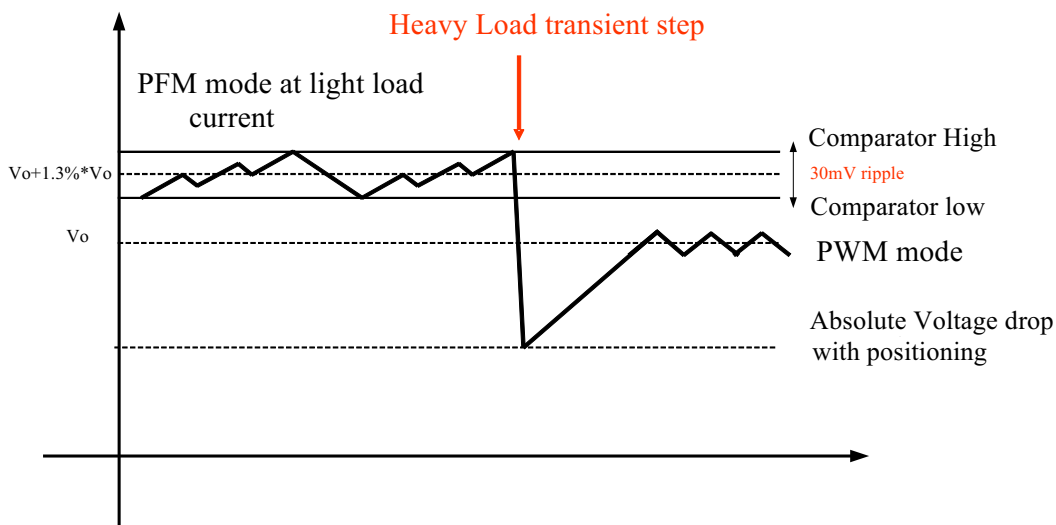


Figure 13. Power Save Mode Operation

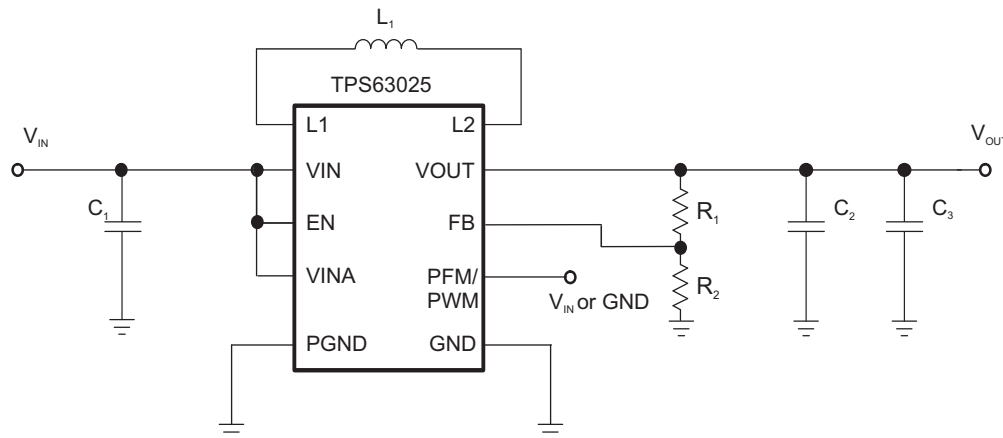
10 Application and Implementation

10.1 Application Information

The devices are designed to operate from an input voltage supply range between 2.3V and 5.5V with a maximum output current of 2A. The TPS63025 device operates in PWM mode for medium to heavy load conditions and in power save mode at light load currents.

In PWM mode the TPS63025 converter operates with the nominal switching frequency of 2.5MHz. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load range.

10.2 Typical Application



10.2.1 Design Requirements

The TPS63025 series of buck-boost converter has internal loop compensation. Therefore, the external LC filter has to be selected according to the internal compensation. Nevertheless, it's important to consider, that the effective inductance, due to inductor tolerance and current derating can vary between +20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -50% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason Table 3 shows the capacitance and inductance value allowed

10.2.2 Detailed Design Procedure

Table 2. List Of Components⁽¹⁾

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63025	Texas Instruments
L1	Shielded, Composite, 1 μ H, 8.75A, 13m Ω ,SMD	XAL4020-102MEB, Colicraft
C1,C2	10 μ F 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C3	CAP, CERM,47 μ F, 6.3V, +/-20%, X5R,0805	GRM219R60J476ME44D, Murata
R1	Depending on the output voltage at adjustable output voltage version, 0 Ω at fixed 3.3V or 2.9V	
R2	Depending on the output voltage at adjustable output voltage version, not used at fixed 3.3V or 2.9V	

(1) See [Third-Party Products Disclaimer](#)

10.2.2.1 Output Filter Design

Table 3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [μH] ⁽¹⁾	NOMINAL OUTPUT CAPACITOR VALUE [μF] ⁽²⁾				
	44	47	66	88	100
0.680			+	+	+
1.0	+(3)	+	+	+	+
1.5			+	+	+

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
 (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
 (3) Typical application. Other check mark indicates recommended filter combinations

10.2.2.2 Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 1. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost } D = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}}} \quad (5)$$

$$I_{\text{PEAK}} = \frac{I_{\text{out}}}{\eta \times (1 - D)} + \frac{V_{\text{in}} \times D}{2 \times f \times L} \quad (6)$$

Where,

D =Duty Cycle in Boost mode

f = Converter switching frequency (typical 2.5MHz)

L = Inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 6. The following inductors are recommended for use:

The inductor value also affects the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means as the inductance and load current increase, the right half plane zero decreases in frequency. This could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >300kHz. The frequency of the RHPZ can be calculated using Equation 7.

$$f_{\text{RHPZ}} = \frac{(1 - D)^2 \times V_{\text{out}}}{2\pi \times I_{\text{out}} \times L} \quad (7)$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Table 4. List of Recommended Inductors⁽¹⁾

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	I _{sat} /DCR
1 μH	Coilcraft XAL4020-102ME	4 X 4 X 2.10	4.5A/10mΩ
1 μH	Toko, DFE322512C	3.2 X 2.5 X 1.2	4.7A/34mΩ
1 μH	TDK, SPM4012	4.4 X 4.1 X 1.2	4.1A/38mΩ
1 μH	Wuerth, 74438334010	3 X 3 X 1.2	6.6A/42.10mΩ
0.6 μH	Coilcraft XFL4012-601ME	4 X 4 X 1.2	5A/17.40mΩ
0.68μH	Wuerth,744383340068	3 X 3 X 1.2	7.7A/36mΩ

(1) See [Third-Party Products Disclaimer](#)

10.2.2.3 Capacitor Selection

10.2.2.3.1 Input Capacitor

At least a 10μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit.

10.2.2.3.2 Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 20μF with a variance as outlined in Table 4.

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

10.2.2.4 Setting The Output Voltage

When the adjustable output voltage version TPS630250 is used, the output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 800mV. The current through the resistive divider should be about 10 times greater than the current into the FB pin. The typical current into the FB pin is 0.1μA, and the voltage across the resistor between FB and GND, R₂, is typically 800 mV. Based on these two values, the recommended value for R₂ should be lower than 180kΩ, in order to set the divider current at 4μA or higher. It is recommended to keep the value for this resistor in the range of 180kΩ. From that, the value of the resistor connected between VOUT and FB, R₁, depending on the needed output voltage (V_{OUT}), can be calculated using [Equation 8](#):

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (8)$$

10.2.3 Application Curves

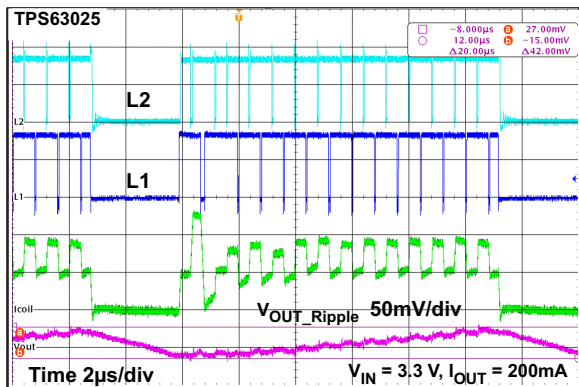


Figure 14. Output Voltage Ripple in Buck-Boost Mode and PFM to PWM Transition

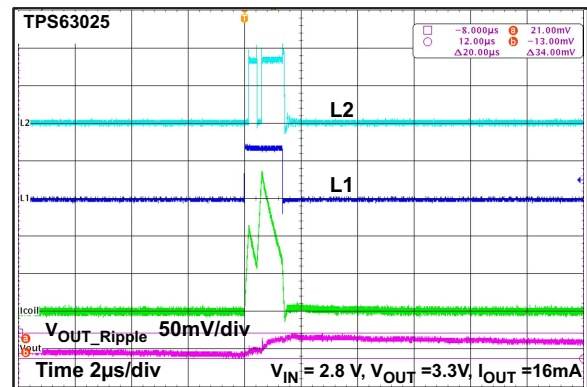


Figure 15. Output Voltage Ripple in Boost Mode and PFM Operation

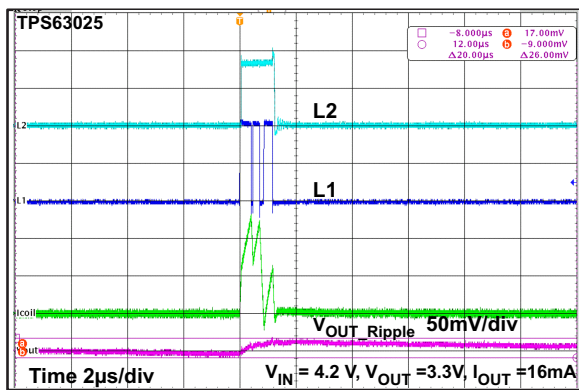


Figure 16. Output Voltage Ripple in Buck Mode and PFM Operation

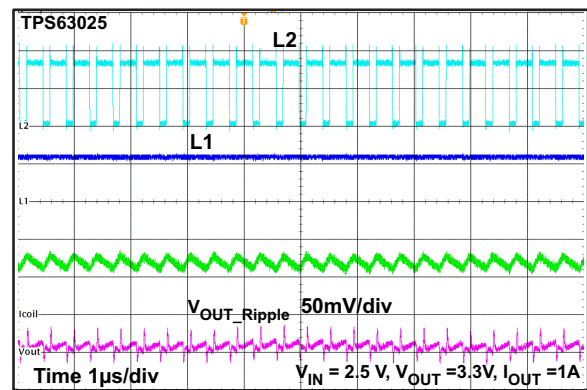


Figure 17. Switching Waveforms in Boost Mode and PWM Operation

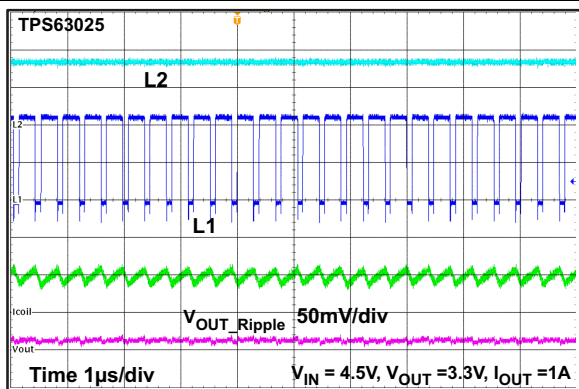


Figure 18. Switching Waveforms in Buck Mode and PWM Operation

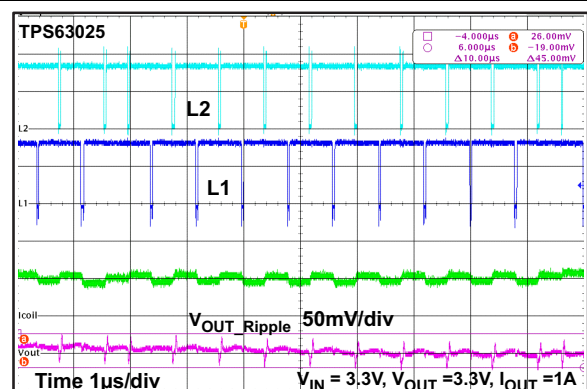


Figure 19. Switching Waveforms in Buck-Boost Mode and PWM Operation

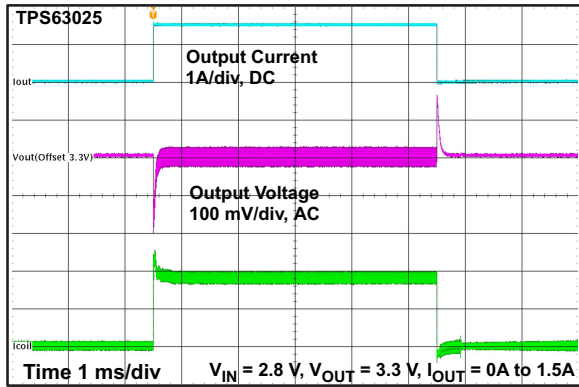


Figure 20. Load Transient Response Boost Mode

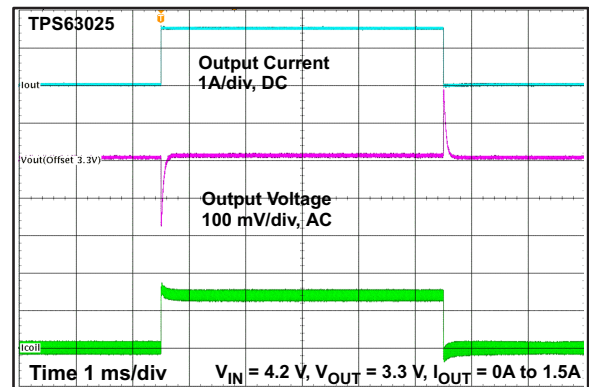


Figure 21. Load Transient Response Buck Mode

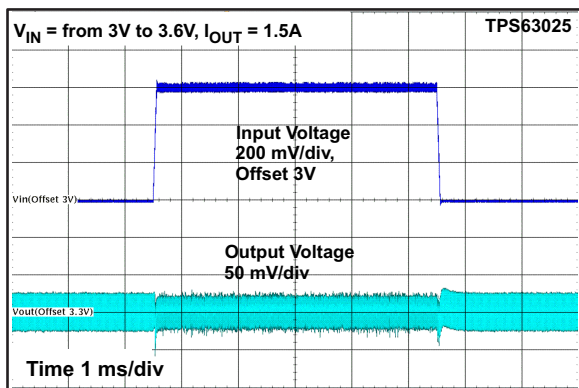


Figure 22. Line Transient Response

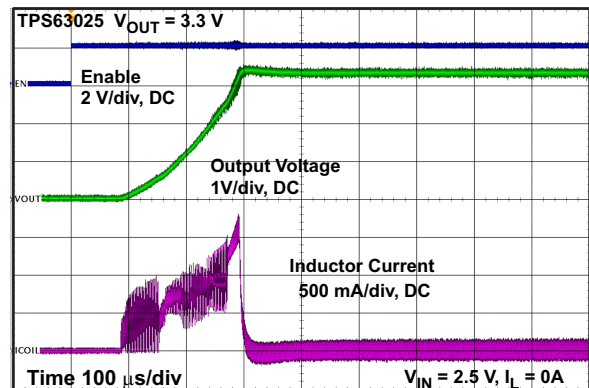


Figure 23. Start Up After Enable

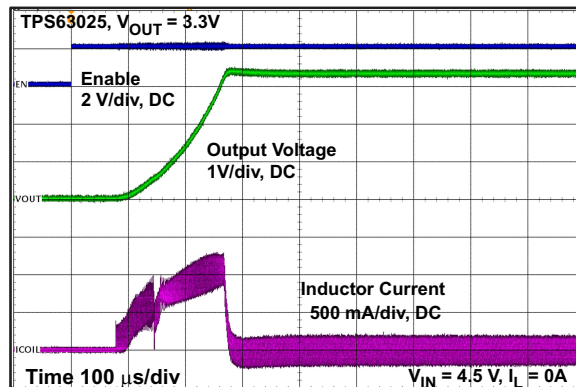


Figure 24. Start Up After Enable

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.3V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS63025 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μ F is a typical choice.

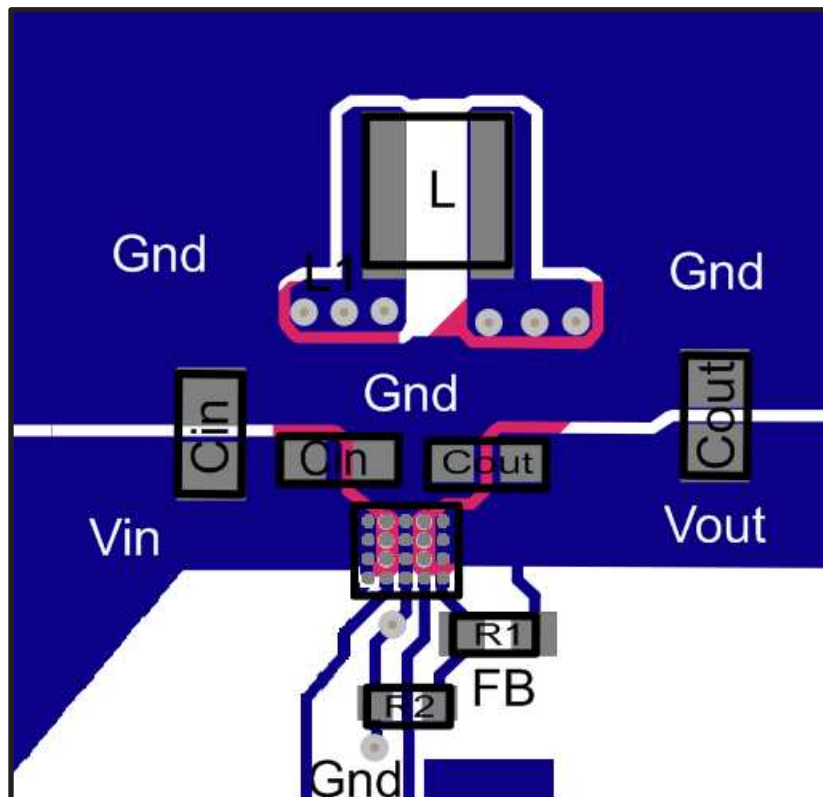
12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63025 devices.

- Place input and output capacitors, along with the inductor, as close as possible to the IC which keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance.
- Use a common-power GND.
- Properly connect the low side of the input and output capacitors to the power GND to avoid a GND potential shift.
- The sense trace connected to FB is signal trace. Keep these trace away from L1 and L2 nodes.
- Use care to avoid noise induction. By a direct routing, parasitic inductance can be kept small.
- Use GND layers for shielding if needed.

12.2 Layout Example



12.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Thermal Information (continued)

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: [Thermal Characteristics Application Note \(SZZA017\)](#), and [IC Package Thermal Metrics Application Note \(SPRA953\)](#).

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

[TPS63025EVM-553 User's Guide](#), [TPS63025 High Current, High Efficiency Single Inductor Buck-Boost Converter](#), [SLVUA24](#)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS630250	Click here	Click here	Click here	Click here	Click here
TPS630251	Click here	Click here	Click here	Click here	Click here
TPS630252	Click here	Click here	Click here	Click here	Click here

13.4 Trademarks

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS630250YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630250	Samples
TPS630250YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630250	Samples
TPS630251YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630251	Samples
TPS630251YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630251	Samples
TPS630252YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630252	Samples
TPS630252YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 630252	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

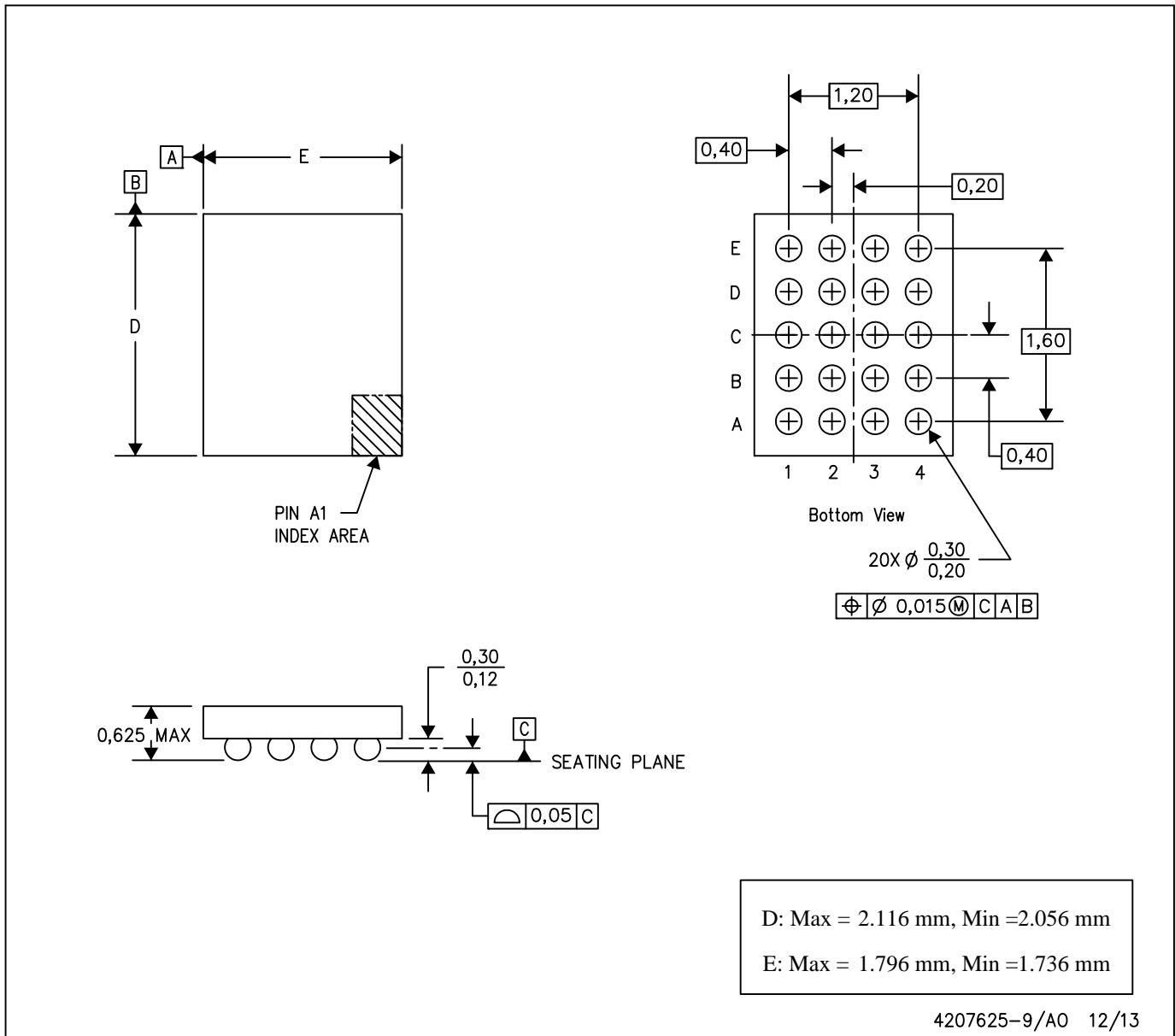
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MECHANICAL DATA

YFF (R-XBGA-N20)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

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